REMARKS

The Examiner is thanked for the thorough examination of the present application. The FINAL Office Action, however, continued to reject all examined claims. Specifically, claims 1, 5, 7, and 10 are rejected under 35 U.S.C. 112. Claims 1, 5, and 10 are rejected under 35 U.S.C. 103(a) as allegely unpatentable over Applicant Admitted Prior Art (AAPA) in view of US 2004/0026741A1 to ***Saito***. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito*** and US 6,376,904 to ***Haba***. Claims 2, 6, 8, and 11 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito*** and US 6,118,310 to ***Esch***. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito***, ***Haba***, and US 6,118,310 to ***Esch***.

In response, Applicant submits the foregoing amendments and the following remarks. Applicant respectfully requests reconsideration and withdrawal of the rejections for at least the reasons set forth herein.

Amendments to the specification

The paragraphs [0007]-[0009], [0019], [0022], [0023], [0026]-[0028] have been amended by replacing the "equivalent impedance" to "impedance" and adding the term "substantially". These amendments add no new matter to the application.

Rejections Under 35 U.S.C. 112

Claims 1, 3, 5, 7, and 10 stand rejected under 35 U.S.C. 112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly clam the subject

matter which Applicant regards as the invention. The Examiner contends that it is not clear how this impedance in measured, and what components of the ESD protection circuit affect this parameter. It is not clear for example whether a connection trace resistance is a part of this impedance.

Applicant submits that there is a specific relationship between impedance and an equivalent channel width of an ESD protection device, and that this relationship is clearly understood by persons of ordinary skill in the art. As described in page 4, lines 20-26 and Fig. 3, an equivalent impedance of the ESD protection device ES_1 is determined according to the channel widths CH1 and CH2, that is, when an equivalent width composed of the channel widths CH1 and CH2 increases, the equivalent impedance of the ESD protection device ES_1 decreases. The specific relationship is an inverter proportion of impedance and an equivalent channel width of an ESD protection device. Thus, when an equivalent channel width of an ESD protection device is obtained, its impedance is also obtained.

Moreover, in the application, the term “impedance” is related to an equivalent channel width of an ESD protection device. The specification clearly describes that the term “impedance” indicates only impedance of an ESD protection device. Thus, a connection trace resistance is a not part of this impedance.

Claim Rejections

Claims 1-2:

Claim 1 is rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito***. Applicant respectfully requests reconsideration and withdrawal of the rejection for at least the following reasons.

Applicant submits that ***Saito*** does not disclose or suggest ESD devices disposed on outermost sides of a connection area having substantially smaller impedance than other ESD protection devices for a plurality of pads. Instead, ***Saito*** discloses a compensation of uneven resistances. According Fig. 8 and paragraph [0037], for one pad 1, the resistances ra of resistors 46a in the area A is higher than the resistance rb of resistors 46b is the area B by a resistance rAB of the parasitic resistance of the signal line 3 from the point A to the point B. Thus, ***Saito*** discloses resistances of resistors in a plurality of areas for one pad.

In contrast, according to claim 1 of prevent application, a plurality of pads (P_1 to P_n) are arranged sequentially, and a plurality of fan-out signal lines (F_1 to F_n) extend from the pads (P_1 to P_n) respectively. The pads P_1 and P_n are disposed on outermost sides of the connection area. A plurality of ESD protection device (ES_1 to ES_n) are configured corresponding to the fan-out signal lines (F_1 to F_n). Impedances of the ESD protection devices ES_1 and ES_n are substantially smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}. In claim 1, in a connection area for a plurality of pads, the impedances of the ESD protection devices ES_1 and ES_n on outermost sides of a connection area are substantially smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}. This feature is not disclosed in ***Saito***.

As demonstrated above, ***Saito*** discloses resistances of resistors for only one pad. In other words, ***Saito*** discloses resistances of resistors as equal to the sum or the total of the resistances of resistors in the area A and the resistances of resistors in the area B, so that ***Saito*** discloses one pad by one resistances of resistors include the area A and the area B. ***Saito*** does not disclose variation of impedances of the ESD protection devices for a plurality of pads in a connection area, especially, relationship between impedances of the ESD protection devices according to their positions in a connection area. Thus, the combination of AAPA and ***Saito*** does not result in the invention of claim 1. Therefore, claim1 patently defines over the cited art, and the rejection of claim 1 should be withdrawn.

As claim 1 is allowable, claim 2, depending from claim 1 and including every claimed element thereof, is also allowable on its own merits in claiming additional elements not included in claim 1.

Claims 3-4:

Claim 3 is rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito*** and ***Haba***. Applicant respectfully traverses the 35 U.S.C. 103(a) rejections for at least the following reason.

Applicant submits that neither ***Saito*** nor ***Haba*** disclose or suggest ESD protection devices having impedances gradually increasing from one outermost ESD protection device to some intermediate ESD protection device and decreasing from there to another outermost ESD protection device.

According to Fig. 4A of ***Haba***, it only relevantly shows shapes of connections between the external terminals and die. Although these connections are configured in a fan-out form, ***Haba*** does not teach that these connections of the fan-out form are applied in ESD protection devices and does not teach the relationship between the length from each ESD protection device to the corresponding pad and impedances of ESD protection devices.

Saito discloses a compensation of uneven resistances. According Fig. 8 and paragraph [0037], for one pad 1, the resistances ra of resistors 46a in the area A is higher than the resistance rb of resistors 46b is the area B by a resistance rAB of the parasitic resistance of the signal line 3 from the point A to the point B. ***Saito*** discloses resistances of resistors in a plurality of areas for one pad. Thus, ***Saito*** discloses resistances of resistors for only one pad. In other words, ***Saito*** discloses resistances of resistors is equal to the sum or the total of the resistances of resistors in the area A and the resistances of resistors in the area B, so that ***Saito*** discloses one pad by resistances of resistors include the area A and the area B. ***Saito*** does not disclose variation of impedances of the ESD protection devices for a plurality of pads in a connection area, especially, relationship between impedances of the ESD protection devices according to their positions in a connection area.

In contrast, according to claim 3, a plurality of pads (P_1 to P_n) are arranged sequentially, and a plurality of fan-out signal lines (F_1 to F_n) extend from the pads (P_1 to P_n) respectively. The pads P_1 and P_n are disposed on outermost sides of the connection area. A plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n). Equivalent-impedances of the ESD

protection devices ES_1 to ES_j gradually increase and equivalent impedances of the ESD protection devices ES_{j+1} to ES_n gradually decrease ($1 < j < n$). In claim 3, in a connection area for a plurality of pads, impedances of ESD protection devices increase from one outermost ESD protection device to some intermediate ESD protection device and decrease from there to another outermost ESD protection device. This feature is not disclosed in ***Saito*** or ***Haba***.

Thus, the combination of AAPA, ***Sait***, and ***Haba*** does not result in the invention of claim 3. AAPA, ***Sait***, and ***Haba*** neither disclose nor suggest, singly, or in combination, the invention of claim 3, and claim 3 defines over the cited art for at least this reason. As claim 3 is allowable, claim 4, depending from claim 3 and including every claimed element thereof, is also allowable on its own merits in claiming additional elements not included in claim 3.

Claims 5-6:

Claim 5 is rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito***. Applicant respectfully requests reconsideration of the rejections for at least the following reason.

Applicant submits that ***Saito*** does not disclose or suggest an impedance of one ESD protection device is substantially different from impedances of the other ESD protection devices for a plurality of pads. ***Saito*** discloses a compensation of uneven resistances is disclosed. According Fig. 8 and paragraph [0037], for one pad 1, the resistances ra of resistors 46a in the area A is higher than the resistance rb of resistors 46b is the area B by a resistance rAB of the parasitic resistance of the signal line 3 from

the point A to the point B. ***Saito*** discloses resistances of resistors in a plurality of areas for one pad.

In contrast, claim 5 recites a plurality of pads (P_1 to P_n) are arranged sequentially, and a plurality of fan-out signal lines (F_1 to F_n) extend from the pads (P_1 to P_n) respectively. The pads P_1 and P_n are disposed on outermost sides of the connection area. A plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n). An impedance of one ESD protection device ES_k is substantially different from impedances of the other ESD protection devices ($1 \leq k \leq n$). In claim 5, in a connection area, for a plurality of pads, the impedance of any one ESD protection device is substantially different from any other ESD protection device. This feature is not disclosed in ***Saito***.

As demonstrated above, ***Saito*** discloses resistances of resistors for only one pad. In other words, ***Saito*** discloses resistances of resistors is equal to the sum or the total of the resistances of resistors in the area A and the resistances of resistors in the area B, so that ***Saito*** discloses one pad by one resistances of resistors include the area A and the area B. ***Saito*** does not disclose impedances of ESD protection devices for a plurality of pads, especially, relationship between impedance of one ESD protection device and that of other ESD protection devices in a connection area. Thus, the combination of AAPA and ***Saito*** does not result in the invention of claim 5. AAPA and ***Saito*** neither disclose nor suggest, singly, or in combination, the invention of claim 5.

Therefore, claim 5 patently defines over the cited art, and the rejections of claim 5 should be withdrawn. As claim 5 is allowable, claim 6, depending from claim 5 and

including every claimed element thereof, is also allowable on their own merits in claiming additional elements not included in claim 5.

Claims 7-9:

Claim 7 is rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito*** and ***Haba***. Applicant respectfully traverses the 35 U.S.C. 103(a) rejections for at least the following reason.

Applicant submits that neither ***Saito*** nor ***Haba*** disclose or suggest ESD devices disposed on outermost sides of a connection area having substantially smaller impedance than other ESD protection devices for a plurality of pads.

According to Fig. 4A of ***Haba***, it only relevantly shows shapes of connections between the external terminals and die. Although these connections are configured as a fan-out form, ***Haba*** does not teach that these connections of the fan-out form are applied in ESD protection devices and the relationship between impedances of the ESD protection devices according to their positions in a connection area.

Saito discloses a compensation of uneven resistances. According Fig. 8 and paragraph [0037], for one pad 1, the resistances ra of resistors 46a in the area A is higher than the resistance rb of resistors 46b is the area B by a resistance rAB of the parasitic resistance of the signal line 3 from the point A to the point B. ***Saito*** discloses resistances of resistors in a plurality of areas for one pad. Thus, ***Saito*** discloses resistances of resistors for only one pad. On other words, ***Saito*** discloses resistances of resistors is equal to the sum or the total of the resistances of resistors in the area A and the resistances of resistors in the area B, so that ***Saito*** discloses one pad by

resistances of resistors include the area A and the area B. ***Saito*** does not disclose variation of impedances of the ESD protection devices for a plurality of pads in a connection area, especially, relationship between impedances of the ESD protection devices according to their positions in a connection area.

In contrast, claim 7 recites a plurality of pads (P_1 to P_n) are arranged sequentially, and a plurality of fan-out signal lines (F_1 to F_n) extend from the pads (P_1 to P_n) respectively. The pads P_1 and P_n are disposed on outermost sides of the connection area. A plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n). Impedances of the ESD protection devices ES_1 and ES_n are substantially smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}. In claim 7, in a connection area, for a plurality of pads, the impedances of the ESD protection devices ES_1 and ES_n on outermost sides of a connection area are substantially smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}. This feature is not disclosed in ***Saito*** and ***Haba***.

Thus, the combination of AAPA, ***Sait***, and ***Haba*** does not result in the invention of claim 7. AAPA, ***Sait***, and ***Haba*** neither disclose nor suggest, singly, or in combination, the invention of claim 7. As claim 7 is allowable, claims 8 and 9, all depending from claim 7, including every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 7.

Claims 10-11:

Claim 10 is rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito***. Applicant respectfully traverses the 35 U.S.C. 103(a) rejections for at least the following reasons.

Applicant submits that ***Saito*** does not disclose or suggest an impedance of one ESD protection device being substantially different from impedances of the other ESD protection devices for a plurality of pads. ***Saito*** discloses a compensation of uneven resistances. According Fig. 8 and paragraph [0037], for one pad 1, the resistances ra of resistors 46a in the area A is higher than the resistance rb of resistors 46b is the area B by a resistance rAB of the parasitic resistance of the signal line 3 from the point A to the point B. ***Saito*** discloses resistances of resistors in a plurality of areas for one pad.

In contrast, claim 10 recites, a plurality of pads (P_1 to P_n) are arranged sequentially, and a plurality of fan-out signal lines (F_1 to F_n) extend from the pads (P_1 to P_n) respectively. The pads P_1 and P_n are disposed on outermost sides of the connection area. A plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n). An impedance of one ESD protection device ES_k is substantially different from impedances of the other ESD protection devices ($1 \leq k \leq n$). In claim 10, in a connection area, for a plurality of pads, the impedance of any one ESD protection device is substantially different from any other ESD protection device. This feature is not disclosed in ***Saito***.

As demonstrated above, ***Saito*** discloses resistances of resistors for only one pad. In other words, ***Saito*** discloses resistances of resistors is equal to the sum or the total of the resistances of resistors in the area A and the resistances of resistors in the

area B, so that ***Saito*** discloses one pad by resistances of resistors include the area A and the area B. ***Saito*** does not disclose impedances of ESD protection devices for a plurality of pads, especially, relationship between impedance of one ESD protection device and that of other ESD protection devices in a connection area. Thus, the combination of AAPA and ***Saito*** does not result in the invention of claim 10. AAPA and ***Saito*** neither disclose nor suggest, singly, or in combination, the invention of claim 10.

Therefore, claim 10 patently defines over the cited art, and the rejections of claim 10 should be withdrawn. As claim 10 is allowable, claim 11, depending from claim 10 and including every claimed element thereof, is also allowable on its own merits in claiming additional elements not included in claim 10.

New claims

New claims 12 and 13 depend from claim 10 and further define features thereof. Accordingly, these new claims are allowable at least by virtue of their dependency from claim 10.

Conclusion

For the reasons as described above, Applicant believes that claims 1-13 are allowable in their present form. Withdrawal of the rejections and allowance of the claims are respectfully requested. Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

A credit card authorization is provided herewith to cover the fee associated with the accompanying RCE application. No additional fee is believed to be due in connection with this submission. If, however, any additional fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

By: _____

Daniel R. McClure
Registration No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500